

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



537953

(43) International Publication Date
1 July 2004 (01.07.2004)

PCT

(10) International Publication Number
WO 2004/055893 A1

(51) International Patent Classification⁷: **H01L 23/525**

(21) International Application Number:
PCT/IB2003/005905

(22) International Filing Date:
13 December 2003 (13.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/434,136 16 December 2002 (16.12.2002) US

(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **DONDERO, Richard** [US/US]; 1109 McKay Drive, M/S-41SJ, San Jose, CA 95131 (US). **TROTTER, Doug** [US/US]; 1109 McKay Drive, M/S-41SJ, San Jose, CA 95131 (US).

(74) Common Representative: **KONINKLIJKE PHILIPS ELECTRONICS N.V.**; c/o **LESTER, Shannon**, 1109 McKay Drive, M/S-41SJ, San Jose, CA 95131 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK,

MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

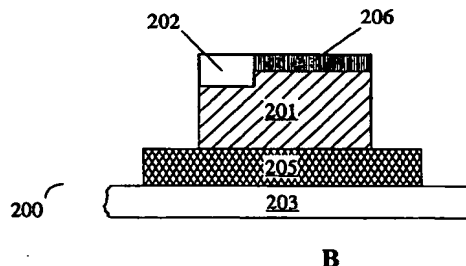
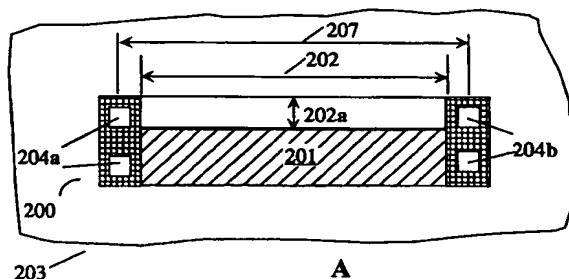
— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

Published:

— with international search report

[Continued on next page]

(54) Title: **POLY-SILICON STRINGER FUSE**



(57) Abstract: A polysilicon silicide stringer fuse is constructed having a narrow width by using an overlay tolerance of the photo stepper tool instead of the minimum critical dimension tolerance of the stepper tool. In an example embodiment, a fuse (200) for integration within a semiconductor comprises depositing an insulating layer (205) adjacent to the semiconductor substrate (203). A silicon layer (201) is formed with a first silicon material having a first resistance deposited adjacent the insulating layer (205). The silicon layer has a first width. A metal silicide stringer (202), having a second resistance different from the first resistance is deposited over a portion of the first silicon material (201) and having a second width that is less than the first width within at least a portion thereof. The metal silicide conducts current therethrough with approximately the second resistance and agglomerates in response to a programming current other than the conduct current therethrough with a same second resistance.

WO 2004/055893 A1